What Is Claimed Is:

1. An electrical circuit comprising:

a low voltage transistor provided in a high voltage environment, said high voltage environment being characterized by a high supply voltage, said low voltage transistor containing a plurality of terminals, said low voltage transistor being designed to operate at a low cross terminal voltage, wherein said low cross terminal voltage is lower than said high supply voltage, one of said plurality of terminals of said low voltage transistor also receiving a voltage at least substantially equaling said high supply voltage.

2. The electrical circuit of claim 1, wherein said low voltage transistor is provided in a path of an input signal being processed by said electrical circuit such that said input signal can be processed quickly.

3. The electrical circuit of claim 2, further comprising a second low voltage transistor provided at an output node of said electrical circuit.

4. The electrical circuit of claim 3, wherein a bulk terminal of said second low voltage transistor is connected to a source terminal of said second low voltage transistor.

5. The electrical circuit of claim 4, wherein said second low voltage transistor comprises a PMOS transistor.

6. The electrical circuit of claim 3, further comprising a third low voltage transistor

having a first terminal connected to said output node, a bulk terminal of said third low voltage transistor being connected to a voltage greater than said low voltage.

7. The electrical circuit of claim 6, wherein a gate terminal of said third low voltage transistor is coupled to a clock signal having a high level greater than or equal to said low voltage.

8. The electrical circuit of claim 7, wherein said high level of said clock signal is substantially more than said low voltage to provide a high drive strength for said third low voltage transistor, and a low level of said clock signal is greater than or equal to (voltage of said high level - a maximum permissible voltage level of said low voltage transistor).

9. The electrical circuit of claim 1, further comprising a clock freeze protect circuit which forces a first node to an acceptable voltage level associated with the operation of said low voltage transistor if a clock signal is stuck at 1 or 0, wherein said first node is also connected to said low voltage transistor.

10. The electrical circuit of claim 9, further comprising:

a capacitor in one of charged or discharged states when said clock signal is not stuck; and

a current source to slowly change said capacitor from said one of charged or discharged states to the other one of said charged or discharged states when said clock signal is stuck.

11. The electrical circuit of claim 10, wherein said clock freeze protect circuit comprises:

a high static sensor determining whether said clock signal is stuck at 1;

a low static sensor determining whether said clock signal is stuck at 0, wherein said low static sensor also comprises said capacitor and said current source;

a logic gate generating a stuck-at signal having a first logical value if either said high static sensor determines that said clock signal is stuck at 1 or if said low static sensor determines that said clock signal is stuck at 0, said stuck-at signal having a second logical value otherwise; and

a fifth transistor, wherein a gate terminal of said fifth transistor is connected to receive said stuck-at signal, another terminal of said fifth transistor is connected to said first node and yet another terminal of said fifth transistor is connected to a reference voltage such that said acceptable voltage level equals said reference voltage.

12. The electrical circuit of claim 11, wherein said fifth transistor comprises a NMOS transistor.

13. The electrical circuit of claim 11, wherein said low static sensor comprises:

a first switch connected between a second node and said high voltage, wherein said first switch turns on in one logical state of said clock signal and turns off on the other logical state of said clock signal;

a second switch connected between said second node and a fourth node, said fourth

node being coupled to ground,

said capacitor provided between said second node and ground, and said current source being connected between said fourth node and ground, wherein said current source generates a desired amount of current to discharge said capacitor slowly; and

an inverter connected to said capacitor at said second node, wherein an output provided by said inverter indicates whether said clock signal is stuck at 0.

14. The electrical circuit of claim 1, further comprising a clamping circuit connected to a first node, wherein said first node is also connected to said low voltage transistor, wherein said clamping circuit is designed to ensure that a voltage level at said first node stays within a specified range.

15. The electrical circuit of claim 14, wherein said clamping circuit comprises:

a high clamping circuit receiving a bias signal and pulling said voltage level at said first node to at least below a maximum permissible voltage level associated with said low voltage transistors if said voltage level at said first node exceeds said maximum permissible voltage level; and

a high clamp biasing circuit generating said bias signal.

16. The electrical circuit of claim 15, wherein said high clamping circuit comprises:

a first transistor designed to be turned on when said voltage level at said first node exceeds said maximum permissible voltage level; and

a first current amplifier drawing a substantial amount of current when said first

transistor is turned on, which causes said voltage level at said first node to be pulled down to said maximum permissible voltage level.

17. The electrical circuit of claim 16, wherein said first transistor comprises a PMOS transistor, wherein a source terminal of said first transistor is connected to said first node, a drain terminal of said first transistor is connected to said current amplifier, and a gate terminal of said first transistor is connected to receive said bias signal from said high clamp biasing circuit, and

said first current amplifier is connected to both of said source terminal and said drain terminal of said first transistor.

18. The electrical circuit of claim 16, wherein said first current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to a drain terminal of said third transistor, a gate terminal of said third transistor receiving a third bias voltage, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to said source terminal of said first transistor.

19. The electrical circuit of claim 18, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

20. The electrical circuit of claim 16, wherein said first current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to each of a drain terminal and a gate terminal of said third transistor, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor.

21. The electrical circuit of claim 20, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

22. The electrical circuit of claim 16, wherein said first current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to both drain and gate terminals of said third transistor, a source terminal of said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor; and

a resistor connected between a source terminal of said third transistor and ground.

23. The electrical circuit of claim 22, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

24. The electrical circuit of claim 15, wherein said high clamp biasing circuit ensures that said bias signal has sufficient strength when said high voltage ramps up.

25. The electrical circuit of claim 24, wherein said high clamp biasing circuit comprises:

a multiplexor receiving a first bias voltage and a second voltage, and providing said second voltage as said bias signal if a selection signal is of a first logical value and said first bias voltage as said bias signal otherwise; and

a comparator generating said selection signal to equal said first logical value if a target voltage generated from said high voltage is below a pre-specified threshold.

26. The electrical circuit of claim 25, wherein said target voltage is designed to ramp up slowest among a plurality of target voltages generated from said high voltage.

27. The electrical circuit of claim 26, wherein said high clamp biasing circuit further comprises a first voltage divider circuit generating said pre-specified threshold as a fraction of said high voltage.

28. The electrical circuit of claim 27, wherein said high clamp biasing circuit further comprises a second voltage divider circuit generating said second voltage as another fraction of said high voltage.

29. The electrical circuit of claim 14, wherein said clamping circuit comprises:

a low clamping circuit receiving a bias signal and ensuring that voltage level at said first node does not fall below another permissible voltage level associated with the operation

of said low voltage transistor; and

a low clamp biasing circuit generating said bias signal.

30. The electrical circuit of claim 29, wherein said low clamping circuit comprises:

a second transistor designed to be turned on when said voltage level at said first node falls below said another permissible voltage level; and

a second current amplifier drawing a substantial amount of current when said second transistor is turned on, which causes said voltage level at said first node to be kept at least at said another permissible voltage level.

31. The electrical circuit of claim 30, wherein said first transistor comprises a NMOS transistor, wherein a source terminal of said second transistor is connected to said first node, a drain terminal of said second transistor is connected to said second current amplifier, and a gate terminal of said second transistor is connected to receive said bias signal from said low clamp biasing circuit, and

said second current amplifier is connected to both of said source terminal and said drain terminal of said second transistor.

32. The electrical circuit of claim 1, further comprising:

a first portion containing a plurality of low voltage transistors, wherein said first portion receives a first supply voltage suitable for operating said low voltage transistors, said first supply voltage being received on a first path;

a second portion generating a biasing signal using a second supply voltage suitable for

said high voltage environment;

a regulator receiving said biasing signal and generating said first supply voltage on said first path based on a third supply voltage; and

a supply sequencing adjusting circuit pulling down voltage level of said first path to an acceptable voltage level for said plurality of low voltage transistors until said second supply voltage ramps up to a pre-specified level.

33. The electrical circuit of claim 32, wherein said supply sequencing adjusting circuit comprises:

a transistor pulling down voltage level of said first path to an acceptable voltage level if a pull down signal is of a first logical value and pulling down voltage level of said first path to said first supply voltage otherwise; and

a comparator generating said pull down signal to equal said first logical value if said second supply voltage is below a pre-specified level.

34. The electrical circuit of claim 33, wherein said supply sequencing adjusting circuit further comprises a voltage divider circuit generating said pre-specified threshold as a fraction of said third supply voltage.

35. A clock freeze protect circuit detecting whether a clock signal is stuck, said clock freeze protect circuit further comprising:

a capacitor in one of charged or discharged states when said clock signal is not stuck; and

a current source to slowly change said capacitor from said one of charged or discharged states to the other one of said charged or discharged states when said clock signal is stuck.

36. The clock freeze protect circuit of claim 35, further comprises:

a high static sensor determining whether said clock signal is stuck at 1;

a low static sensor determining whether said clock signal is stuck at 0, wherein said low static sensor also comprises said capacitor and said current source;

a logic gate generating a stuck-at signal having a first logical value if either said high static sensor determines that said clock signal is stuck at 1 or if said low static sensor determines that said clock signal is stuck at 0, said stuck-at signal having a second logical value otherwise; and

a fifth transistor, wherein a gate terminal of said fifth transistor is connected to receive said stuck-at signal, another terminal of said fifth transistor is connected to said first node and yet another terminal of said fifth transistor is connected to a reference voltage such that said acceptable voltage level equals said reference voltage.

37. The clock freeze protect circuit of claim 36, wherein said fifth transistor comprises a NMOS transistor.

38. The clock freeze protect circuit of claim 36, wherein said low static sensor comprises:

a first switch connected between a second node and said high voltage, wherein said

first switch turns on in one logical state of said clock signal and turns off on the other logical state of said clock signal;

a second switch connected between said second node and a fourth node, said fourth node being coupled to ground,

said capacitor provided between said second node and ground, and said current source being connected between said fourth node and ground, wherein said current source generates a desired amount of current to discharge said capacitor slowly; and

an inverter connected to said capacitor at said second node, wherein an output provided by said inverter indicates whether said clock signal is stuck at 0.

39. An electrical circuit comprising:

a low voltage transistor designed for operation at a low voltage and having a maximum permissible voltage, said low voltage transistor containing a plurality of terminals including a first terminal, said low voltage transistor being connected to a first higher voltage, wherein said first higher voltage is greater than said low voltage, wherein a cross terminal voltage between said first terminal and each of the remaining terminal is constrained to not exceed said maximum permissible voltage.

40. The electrical circuit of claim 39, wherein said first higher voltage comprises a substantial fraction of high supply voltage associated with a high voltage environment.

41. The electrical circuit of claim 40, further comprising a high voltage transistor designed for operation at said high supply voltage.

42. The electrical circuit of claim 41, wherein said low voltage transistor comprises a PMOS transistor, wherein a bulk terminal of said PMOS transistor is connected to a source terminal of said PMOS transistor, wherein both of said bulk terminal and said source terminal are coupled to receive a slightly less voltage than said high supply voltage.

43. The electrical circuit of claim of claim 41, wherein said low voltage transistor comprises a PMOS transistor, wherein a bulk terminal of said PMOS transistor is connected to a voltage slightly higher than said low voltage.

44. The electrical circuit of claim 43, wherein said bulk terminal is connected to 2.1V and said low voltage equals 1.8V.

45. The electrical circuit of claim 41, wherein a source terminal of said low voltage transistor is connected to said high supply voltage, a gate terminal of said low voltage transistor is connected to receive a clock signal having a high level slightly greater than or equal to said low voltage.

46. The electrical circuit of claim 45, wherein said low voltage transistor comprises a NMOS transistor, wherein said high level of said clock signal is substantially more than said low voltage to provide a high drive strength for said low voltage transistor, and a low level of said clock signal is greater than or equal to (voltage of said high level - a maximum permissible voltage level of said low voltage transistor).

47. The electrical circuit of claim 46, wherein said low voltage equals 1.8V, said maximum permissible voltage equals 2.4V, said high level equals 2.5V, and said low voltage equals 0.5V.

48. An electrical circuit comprising:

a low voltage transistor designed for operation at a low voltage, said low voltage transistor comprising a plurality of terminals including a first terminal and a second terminal, a higher voltage being applied on said first terminal, wherein said higher voltage is greater than said low voltage; and

a clamping circuit ensuring that a voltage level on a path coupled to said second terminal is within a specified range to avoid damaging said low voltage transistor.

49. The electrical circuit of claim 48, wherein said low voltage transistor is provided in a high voltage environment.

50. The electrical circuit of claim 49, wherein said low voltage equals 1.8V and said specified range equals 0.6V to 2.4V.

51. An electrical circuit comprising:

a low voltage NMOS transistor designed for operation at a low voltage, a gate terminal of said low voltage NMOS transistor being connected to a clock signal having a high level greater than said low voltage to provide a high drive strength to said low voltage NMOS

transistor.

52. The electrical circuit of claim 51, wherein said low voltage NMOS transistor is characterized by a maximum permissible voltage, wherein said high level is greater than said maximum permissible voltage.

53. The electrical circuit of claim 52, further comprising a clock generator for generating said clock signal, said clock generator comprising an inverter, said inverter comprising a second low voltage NMOS transistor and a second low voltage PMOS transistor, wherein said high level is provided on a source terminal of said second low voltage PMOS transistor and a voltage equaling a low level of said clock signal is provided on a source terminal of said second low voltage NMOS transistor, wherein said low level is greater than or equal to (voltage of said high level - a maximum permissible voltage level of said low voltage transistor) to ensure that cross terminal voltages in each of said second low voltage NMOS transistor and said second low voltage PMOS transistor is in an acceptable range.

54. An electrical circuit comprising:

a first portion implemented as a high voltage environment and receiving a clock signal, said first portion containing a low voltage transistor designed for operation at a low voltage; and

a clock freeze protect circuit ensuring that a voltage level on a path coupled to said first portion is within an acceptable voltage level if said clock signal is stuck.

55. The electrical circuit of claim 54, wherein said clock freeze protect circuit comprises:

a capacitor in one of charged or discharged states when said clock signal is not stuck; and

a current source to slowly change said capacitor from said one of charged or discharged states to the other one of said charged or discharged states when said clock signal is stuck.

56. The electrical circuit of claim 55, wherein said first portion comprises a sample and hold amplifier (SHA), wherein said clock freeze protect circuit tri-states said SHA if said clock signal is stuck.

57. An electrical circuit comprising:

a first portion implemented as a high voltage environment and receiving an input signal, said first portion containing a low voltage transistor designed for operation at a low voltage;

a bandgap circuit generating a plurality of target voltages based on a high supply voltage, said plurality of target voltages comprising a first target voltage; and

a selection circuit receiving said first target voltage, and providing a first voltage derived from said high supply voltage as said input signal when said first target signal is ramping up, said selection circuit providing a signal generated from said first target voltage as said input signal after said first target signal has substantially ramped up.

58. The electrical circuit of claim 57, further comprising:

a clamping circuit which ensures that the voltage of a path in said first portion is within a specified range, wherein said input signal is provided as a bias signal to said clamping circuit.

59. The electrical circuit of claim 58, wherein said selection circuit comprises a comparator which compares a slow one of said plurality of target voltages with a voltage derived from said high supply voltage.

60. The electrical circuit of claim 59, wherein said high supply voltage equals 3.3V and said low voltage equals 1.8V.

61. An electrical circuit comprising:

a first portion containing a plurality of low voltage transistors, wherein said first portion receives a first supply voltage suitable for operating said low voltage transistors, said first supply voltage being received on a first path;

a second portion generating a biasing signal using a second supply voltage suitable for a high voltage environment;

a regulator receiving said biasing signal and generating said first supply voltage on said first path based on a third supply voltage; and

a supply sequencing adjusting circuit pulling down voltage level of said first path to an acceptable voltage level for said plurality of low voltage transistors until said second supply voltage ramps up to a pre-specified level.

62. The electrical circuit of claim 61, wherein said supply sequencing adjusting circuit comprises:

a transistor pulling down voltage level of said first path to an acceptable voltage level if a pull down signal is of a first logical value and pulling down voltage level of said first path to said first supply voltage otherwise; and

a comparator generating said pull down signal to equal said first logical value if said second supply voltage is below a pre-specified level.

63. The electrical circuit of claim 62, wherein said supply sequencing adjusting circuit further comprises a voltage divider circuit generating said pre-specified threshold as a fraction of said third supply voltage.

64. The electrical circuit of claim 62, wherein said supply sequencing adjustment circuit tri-states said regulator if said pull-down signal is of said first logical value.

65. A device comprising:

a low voltage transistor in a high voltage environment, wherein said high voltage environment is characterized by a high supply voltage and a voltage equaling said high supply voltage is applied to one of the terminals of said low voltage transistor; and

means for constraining cross terminal voltages of said low voltage transistor to substantially less than a maximum permissible voltage for which said low voltage transistor is designed, wherein said maximum permissible voltage is less than said high supply voltage.

66. The device of claim 65, wherein said means for constraining does not contain a low voltage regulator which generates said low voltage from said high voltage.

67. The device of claim 65, wherein said cross terminal voltages are constrained to not substantially more than a low voltage for which said low voltage transistor is designed.

68. A device comprising:

a voltage source providing a high supply voltage;

a low voltage transistor comprising a plurality of terminals; and

means for clamping the voltage at a path coupled to one of said plurality of terminals to a specified range such that none of the cross terminal voltages of said low voltage transistor exceeds a low voltage for which said low voltage transistor is designed for.

69. The device of claim 68, wherein said means for clamping receives a bias voltage, said device further comprising:

means for ensuring that said bias voltage is at least at a pre-specified voltage level when said high supply voltage is ramping up.

70. The device of claim 69, wherein said means for ensuring is operable to:

generate a plurality of target voltages based on said high supply voltage, said plurality of target voltages comprising a first target voltage;

provide a first voltage derived from said high supply voltage as said bias voltage when

said first target signal is ramping up; and

provide a signal generated from said first target voltage as said bias voltage after said first target signal has substantially ramped up.

71. A device comprising:

a voltage source providing a high supply voltage;

a low voltage transistor contained in a portion of an electrical circuit, wherein said portion receives a clock signal;

means for detecting whether said clock signal is stuck; and

means for pulling a voltage level at a node to an acceptable voltage level associated with the operation of said low voltage transistor if said clock signal is stuck, wherein said node is coupled to one of the terminals of said low voltage transistor.

72. The device of claim 71, wherein said portion comprises a sample and hold amplifier (SHA), said device further comprising means for tri-stating said SHA if said clock signal is detected to be stuck.

73. A device of implementing an device, said device comprising:

using a high supply voltage for said device;

providing a low voltage transistor in said device, wherein said low voltage transistor is designed to operate at a low voltage which is less than said high supply voltage, wherein a first terminal of said low voltage transistor receives a clock signal;

setting a high level of said clock signal to have a voltage greater than said low voltage

to provide a high drive strength to said low voltage transistor.

74. The device of claim 73, further comprising setting a low level of said clock signal to have a voltage greater than or equal to (voltage of said high level - a maximum permissible voltage level of said low voltage transistor).

75. The device of claim 74, wherein said low voltage transistor comprises a NMOS transistor.

76. The device of claim 75, wherein said first terminal comprises a gate terminal.

77. A device comprising:

a low voltage transistor provided in a high voltage environment, said high voltage environment being characterized by a high supply voltage, said low voltage transistor containing a plurality of terminals, said low voltage transistor being designed to operate at a low cross terminal voltage, wherein said low cross terminal voltage is lower than said high supply voltage, one of said plurality of terminals of said low voltage transistor also receiving a voltage at least substantially equaling said high supply voltage.

78. The device of claim 77, wherein said low voltage transistor is provided in a path of an input signal being processed by said device such that said input signal can be processed quickly.

79. The device of claim 78, further comprising a second low voltage transistor provided at an output node of an electrical circuit contained in said device.

80. The device of claim 79, wherein a bulk terminal of said second low voltage transistor is connected to a source terminal of said second low voltage transistor.

81. The device of claim 80, wherein said second low voltage transistor comprises a PMOS transistor.

82. The device of claim 79, further comprising a third low voltage transistor having a first terminal connected to said output node, a bulk terminal of said third low voltage transistor being connected to a voltage greater than said low voltage.

83. The device of claim 82, wherein a gate terminal of said third low voltage transistor is coupled to a clock signal having a high level greater than or equal to said low voltage.

84. The device of claim 83, wherein said high level of said clock signal is substantially more than said low voltage to provide a high drive strength for said third low voltage transistor, and a low level of said clock signal is greater than or equal to (voltage of said high level - a maximum permissible voltage level of said low voltage transistor).

85. The device of claim 77, further comprising a clock freeze protect circuit which forces a first node to an acceptable voltage level associated with the operation of said low

voltage transistor if a clock signal is stuck at 1 or 0, wherein said first node is also connected to said low voltage transistor.

86. The device of claim 85, further comprising:

a capacitor in one of charged or discharged states when said clock signal is not stuck; and

a current source to slowly change said capacitor from said one of charged or discharged states to the other one of said charged or discharged states when said clock signal is stuck.

87. The device of claim 86, wherein said clock freeze protect circuit comprises:

a high static sensor determining whether said clock signal is stuck at 1;

a low static sensor determining whether said clock signal is stuck at 0, wherein said low static sensor also comprises said capacitor and said current source;

a logic gate generating a stuck-at signal having a first logical value if either said high static sensor determines that said clock signal is stuck at 1 or if said low static sensor determines that said clock signal is stuck at 0, said stuck-at signal having a second logical value otherwise; and

a fifth transistor, wherein a gate terminal of said fifth transistor is connected to receive said stuck-at signal, another terminal of said fifth transistor is connected to said first node and yet another terminal of said fifth transistor is connected to a reference voltage such that said acceptable voltage level equals said reference voltage.

88. The device of claim 87, wherein said fifth transistor comprises a NMOS transistor.

89. The device of claim 87, wherein said low static sensor comprises:

a first switch connected between a second node and said high voltage, wherein said first switch turns on in one logical state of said clock signal and turns off on the other logical state of said clock signal;

a second switch connected between said second node and a fourth node, said fourth node being coupled to ground,

said capacitor provided between said second node and ground, and said current source being connected between said fourth node and ground, wherein said current source generates a desired amount of current to discharge said capacitor slowly; and

an inverter connected to said capacitor at said second node, wherein an output provided by said inverter indicates whether said clock signal is stuck at 0.

90. The device of claim 77, further comprising a clamping circuit connected to a first node, wherein said first node is also connected to said low voltage transistor, wherein said clamping circuit is designed to ensure that a voltage level at said first node stays within a specified range.

91. The device of claim 90, wherein said clamping circuit comprises:

a high clamping circuit receiving a bias signal and pulling said voltage level at said first node to at least below a maximum permissible voltage level associated with said low voltage transistors if said voltage level at said first node exceeds said maximum permissible

voltage level; and

a high clamp biasing circuit generating said bias signal.

92. The device of claim 91, wherein said high clamping circuit comprises:

a first transistor designed to be turned on when said voltage level at said first node exceeds said maximum permissible voltage level; and

a first current amplifier drawing a substantial amount of current when said first transistor is turned on, which causes said voltage level at said first node to be pulled down to said maximum permissible voltage level.

93. The device of claim 92, wherein said first transistor comprises a PMOS transistor, wherein a source terminal of said first transistor is connected to said first node, a drain terminal of said first transistor is connected to said current amplifier, and a gate terminal of said first transistor is connected to receive said bias signal from said high clamp biasing circuit, and

said first current amplifier is connected to both of said source terminal and said drain terminal of said first transistor.

94. The device of claim 92, wherein said first current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to a drain terminal of said third transistor, a gate terminal of said third transistor receiving a third bias voltage, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is

connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to said source terminal of said first transistor.

95. The device of claim 94, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

96. The device of claim 92, wherein said first current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to each of a drain terminal and a gate terminal of said third transistor, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor.

97. The device of claim 96, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

98. The device of claim 92, wherein said first current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to both drain and gate terminals of said third transistor, a source terminal of said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor; and

a resistor connected between a source terminal of said third transistor and ground.

99. The device of claim 98, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

100. The device of claim 91, wherein said high clamp biasing circuit ensures that said bias signal has sufficient strength when said high voltage ramps up.

101. The device of claim 100, wherein said high clamp biasing circuit comprises:

a multiplexor receiving a first bias voltage and a second voltage, and providing said second voltage as said bias signal if a selection signal is of a first logical value and said first bias voltage as said bias signal otherwise; and

a comparator generating said selection signal to equal said first logical value if a target voltage generated from said high voltage is below a pre-specified threshold.

102. The device of claim 101, wherein said target voltage is designed to ramp up slowest among a plurality of target voltages generated from said high voltage.

103. The device of claim 102, wherein said high clamp biasing circuit further comprises a first voltage divider circuit generating said pre-specified threshold as a fraction of said high voltage.

104. The device of claim 103, wherein said high clamp biasing circuit further

comprises a second voltage divider circuit generating said second voltage as another fraction of said high voltage.

105. The device of claim 90, wherein said clamping circuit comprises:

a low clamping circuit receiving a bias signal and ensuring that voltage level at said first node does not fall below another permissible voltage level associated with the operation of said low voltage transistor; and

a low clamp biasing circuit generating said bias signal.

106. The device of claim 105, wherein said low clamping circuit comprises:

a second transistor designed to be turned on when said voltage level at said first node falls below said another permissible voltage level; and

a second current amplifier drawing a substantial amount of current when said second transistor is turned on, which causes said voltage level at said first node to be kept at least at said another permissible voltage level.

107. The device of claim 106, wherein said first transistor comprises a NMOS transistor, wherein a source terminal of said second transistor is connected to said first node, a drain terminal of said second transistor is connected to said second current amplifier, and a gate terminal of said second transistor is connected to receive said bias signal from said low clamp biasing circuit, and

said second current amplifier is connected to both of said source terminal and said drain terminal of said second transistor.

108. The device of claim 77, further comprising:

a first portion containing a plurality of low voltage transistors, wherein said first portion receives a first supply voltage suitable for operating said low voltage transistors, said first supply voltage being received on a first path;

a second portion generating a biasing signal using a second supply voltage suitable for said high voltage environment;

a regulator receiving said biasing signal and generating said first supply voltage on said first path based on a third supply voltage; and

a supply sequencing adjusting circuit pulling down voltage level of said first path to an acceptable voltage level for said plurality of low voltage transistors until said second supply voltage ramps up to a pre-specified level.

109. The device of claim 108, wherein said supply sequencing adjusting circuit comprises:

a transistor pulling down voltage level of said first path to an acceptable voltage level if a pull down signal is of a first logical value and pulling down voltage level of said first path to said first supply voltage otherwise; and

a comparator generating said pull down signal to equal said first logical value if said second supply voltage is below a pre-specified level.

110. The device of claim 109, wherein said supply sequencing adjusting circuit further comprises a voltage divider circuit generating said pre-specified threshold as a fraction

of said third supply voltage.

111. The device of claim 110, further comprises:

an analog to digital converter comprising a plurality of low voltage transistors, wherein said plurality of low voltage transistors comprises said low voltage transistor.

112. The device of claim 111, wherein said device comprises a wireless base station, said device further comprising:

an antenna receiving an external signal; and

an analog processor processing said external signal to generate said input signal.

113. A method of implementing an electrical circuit, said method comprising:

providing a low voltage transistor in a high voltage environment, wherein said high voltage environment is characterized by a high supply voltage and a voltage equaling said high supply voltage is applied to one of the terminals of said low voltage transistor; and

constraining cross terminal voltages of said low voltage transistor to substantially less than a maximum permissible voltage for which said low voltage transistor is designed, wherein said maximum permissible voltage is less than said high supply voltage.

114. The method of claim 113, wherein said constraining is performed without using a low voltage regulator which generates said low voltage from said high voltage.

115. The method of claim 113, wherein said cross terminal voltages are constrained

to not substantially more than a low voltage for which said low voltage transistor is designed.

116. A method of implementing an electrical circuit with a high SNR and a high throughput performance, wherein said electrical circuit is designed to process an input signal and generate an output signal, said method comprising:

using a high supply voltage for said electrical circuit; and

providing a low voltage transistor in a path from said input signal to said output signal, wherein said low voltage transistor provides said high throughput performance and wherein said use of high supply voltage enables providing said high SNR.

117. The method of claim 116, wherein said low voltage equals 3.3 V and said high supply voltage equals 1.8V.

118. The method of claim 116, wherein said input signal comprises an analog signal.

119. The method of claim 116, wherein said output signal comprises an analog signal.

120. A method of implementing an electrical circuit, said method comprising:

using a high supply voltage for said electrical circuit; and

providing a low voltage transistor in said electrical circuit, wherein said low voltage transistor is not operated using a low voltage signal generated by a voltage regulator.

121. A method of implementing an electrical circuit, said method comprising:

using a high supply voltage for said electrical circuit;

providing a low voltage transistor in said electrical circuit, wherein said low voltage transistor comprises a plurality of terminals; and

clamping the voltage at a path coupled to one of said plurality of terminals to a specified range such that none of the cross terminal voltages of said low voltage transistor exceeds a low voltage for which said low voltage transistor is designed for.

122. The method of claim 121, wherein a clamping circuit is used to perform said clamping, said clamping circuit receiving a bias voltage, said method further comprising:

ensuring that said bias voltage is at least at a pre-specified voltage level when said high supply voltage is ramping up.

123. The method of claim 122, wherein said ensuring comprises:

generating a plurality of target voltages based on said high supply voltage, said plurality of target voltages comprising a first target voltage;

providing a first voltage derived from said high supply voltage as said bias voltage when said first target signal is ramping up; and

providing a signal generated from said first target voltage as said bias voltage after said first target signal has substantially ramped up.

124. A method of implementing an electrical circuit, said method comprising:

using a high supply voltage for said electrical circuit;

providing a low voltage transistor in said electrical circuit, wherein at least a portion

of said electrical circuit receives a clock signal;

detecting whether said clock signal is stuck; and

pulling a voltage level at a node to an acceptable voltage level associated with the operation of said low voltage transistor if said clock signal is stuck, wherein said node is coupled to one of the terminals of said low voltage transistor.

125. The method of claim 124, wherein said portion comprises a sample and hold amplifier (SHA), said method further comprising tri-stating said SHA if said clock signal is detected to be stuck.

126. A method of implementing an electrical circuit, said method comprising:

using a high supply voltage for said electrical circuit;

providing a low voltage transistor in said electrical circuit, wherein said low voltage transistor is designed to operate at a low voltage which is less than said high supply voltage, wherein a first terminal of said low voltage transistor receives a clock signal;

setting a high level of said clock signal to have a voltage greater than said low voltage to provide a high drive strength to said low voltage transistor.

127. The method of claim 126, further comprising setting a low level of said clock signal to have a voltage greater than or equal to (voltage of said high level - a maximum permissible voltage level of said low voltage transistor).

128. The method of claim 127, wherein said low voltage transistor comprises a

NMOS transistor.

129. The method of claim 128, wherein said first terminal comprises a gate terminal.

130. A method of implementing an electrical circuit, said method comprising:

including a plurality of low voltage transistors in a first portion, wherein said first portion receives a first supply voltage suitable for operating said low voltage transistors, said first supply voltage being received on a first path;

generating a biasing signal using a second supply voltage suitable for a high voltage environment;

generating said first supply voltage on said first path based on a third supply voltage and said biasing signal;

determining whether said second supply voltage is ramped up to a pre-specified level; and

pulling down a voltage level of said first path to an acceptable voltage level for said plurality of low voltage transistors until said second supply voltage ramps up to said pre-specified level.

131. A high clamping circuit ensuring that a voltage level at a node is below an upper limit, said high clamping circuit comprising:

a NMOS transistor drawing a substantial amount of current from said node when said voltage level at said node is greater than or equal to said upper limit.

132. The high clamping circuit of claim 131, further comprising a PMOS transistor which is turned on when said voltage level at said node is greater than or equal to said upper limit, wherein turning on of said PMOS transistor causes said NMOS transistor to draw said substantial amount of current.

133. A clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range; and

a current amplifier drawing a substantial amount of current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range.

134. The clamping circuit of claim 133, further comprising a biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range.

135. The clamping circuit of claim 134, wherein said first transistor and said current amplifier are contained in a high clamping circuit which clamps said voltage to said upper limit of said specified range, wherein said voltage level of said bias signal is determined by said upper limit,

wherein said first transistor comprises a PMOS transistor, wherein a source terminal of said first transistor is connected to said node, a drain terminal of said first transistor is

connected to said current amplifier, and

said current amplifier is connected to both of said source terminal and said drain terminal of said first transistor.

136. The clamping circuit of claim 134, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to a drain terminal of said third transistor, a gate terminal of said third transistor receiving a third bias voltage, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to said source terminal of said first transistor.

137. The clamping circuit of claim 136, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

138. The clamping circuit of claim 134, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to each of a drain terminal and a gate terminal of said third transistor, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor.

139. The clamping circuit of claim 138, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

140. The clamping circuit of claim 134, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to both drain and gate terminals of said third transistor, a source terminal of said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor; and

a resistor connected between a source terminal of said third transistor and ground.

141. The clamping circuit of claim 140, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

142. The clamping circuit of claim 134, wherein said first transistor and said current amplifier are contained in a low clamping circuit which clamps said voltage to said lower limit of said specified range, wherein said voltage level of said bias signal is determined by said lower limit, wherein said first transistor comprises a NMOS transistor, wherein a source terminal of said first transistor is connected to said node, a drain terminal of said first transistor is connected to said current amplifier, and said current amplifier is connected to both of said source terminal and said drain terminal of said first transistor.

143. A device comprising:

a high clamping circuit ensuring that a voltage level at a node is below an upper limit, said high clamping circuit comprising a NMOS transistor drawing a substantial amount of current from said node when said voltage level at said node is greater than or equal to said upper limit.

144. The device of claim 143, further comprising a PMOS transistor which is turned on when said voltage level at said node is greater than or equal to said upper limit, wherein turning on of said PMOS transistor causes said NMOS transistor to draw said substantial amount of current.

145. A device comprising:

a clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range; and

a current amplifier drawing a substantial amount of current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range.

146. The device of claim 145, wherein said clamping circuit further comprises a biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range.

147. The device of claim 146, wherein said first transistor and said current amplifier are contained in a high clamping circuit which clamps said voltage to said upper limit of said specified range, wherein said voltage level of said bias signal is determined by said upper limit,

wherein said first transistor comprises a PMOS transistor, wherein a source terminal of said first transistor is connected to said node, a drain terminal of said first transistor is connected to said current amplifier, and

said current amplifier is connected to both of said source terminal and said drain terminal of said first transistor.

148. The device of claim 146, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to a drain terminal of said third transistor, a gate terminal of said third transistor receiving a third bias voltage, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to said source terminal of said first transistor.

149. The device of claim 148, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

150. The device of claim 146, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to each of a drain terminal and a gate terminal of said third transistor, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor.

151. The device of claim 150, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

152. The device of claim 146, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to both drain and gate terminals of said third transistor, a source terminal of said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor; and

a resistor connected between a source terminal of said third transistor and ground.

153. The device of claim 152, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

154. The device of claim 146, wherein said first transistor and said current amplifier are contained in a low clamping circuit which clamps said voltage to said lower limit of said

specified range, wherein said voltage level of said bias signal is determined by said lower limit, wherein said first transistor comprises a NMOS transistor, wherein a source terminal of said first transistor is connected to said node, a drain terminal of said first transistor is connected to said current amplifier, and said current amplifier is connected to both of said source terminal and said drain terminal of said first transistor.

155. The device of claim 154, wherein said device comprises a wireless base station, said device further comprising:

an antenna receiving an external signal; and

an analog processor processing said external signal.